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(54) Voltage regulator with voltage drop compensation for a programming circuitry of non-volatile electrically programmable memory cells

(57) The invention relates to a compensated voltage regulator (1) useful with programming circuitry for electrically programmable non-volatile memory cells in a cell matrix (3) which is divided in sectors (7), the regulator being of a type which includes a comparator (2) connected between first (V_{pp}) and second (GND) supply voltage references, and having:

a first input terminal (+) which is supplied by a reference voltage (V_{ref});

an output terminal (U) connected to the control terminal of an output MOS transistor (M_{cas}) having a conduction terminal through which an output current (I_{out}) is passed and being connected to the

memory cells by a program line (10);

a second input terminal (-), feedback connected to said program line (10).

A compensation block (20) is provided which is powered from said first voltage reference (V_{pp}) and has an input connected to both said output terminal (U) and said output transistor (M_{cas}), and has an output connected to said output terminal (U) to duplicate a current (I_{out}·α) which is suitably attenuated with respect to the output current (I_{out}) and useful to modify the output voltage (V_g) of the comparator (2) included in the regulator.

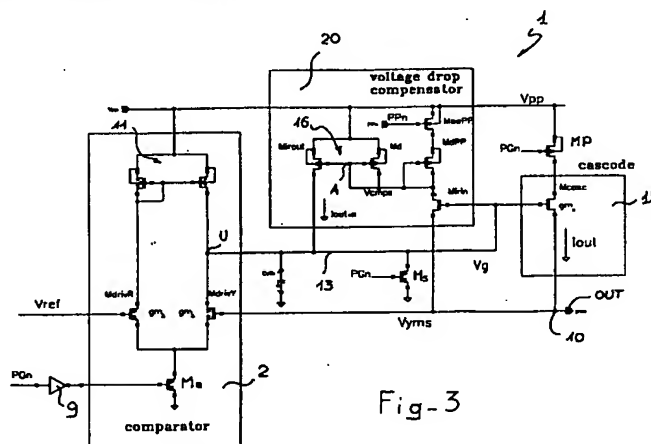


Fig-3

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Description

Field of the Invention

[0001] This invention relates to a voltage regulator for suitably biasing the terminals of electrically programmable non-volatile memory cells.

[0002] In particular, the invention relates to a compensated voltage regulator useful with programming circuitry for electrically programmable non-volatile memory cells in a cell matrix which is divided in sectors, said regulator being of a type which includes a comparator connected between first and second supply voltage references, and having:

a first input terminal which is supplied by a reference voltage;

an output terminal connected to the control terminal of an output MOS transistor having a conduction terminal through which an output current is passed and being connected to the memory cells by a program line;

a second input terminal, feedback connected to said program line.

[0003] As is well known, electrically programmable non-volatile memories are constructed as matrices of memory cells, each comprised of a floating-gate MOS transistor with respective drain and source regions.

[0004] The floating gate is formed over the semiconductor substrate and is isolated from the latter by a thin layer of gate oxide. A control gate is coupled capacitively through a dielectric layer to the floating gate. Metal electrodes are provided for contacting the drain, source, and control gate in order for predetermined value voltages to be applied to the memory cell.

[0005] By suitably biasing the cell terminals, the amount of charge present on the floating gate can be varied. The operation whereby charge is stored up in the floating gate is called "programming", and consists of biasing the drain terminal and the control gate to a predetermined higher value than the potential at the source terminal.

[0006] A semiconductor-integrated memory device usually includes a very large number of cells of the above-mentioned type. The cells are organized in a matrix formed of rows, or word lines, and columns, or bit lines. All the cells in one word line share a electric drive line for their respective control gates, while the cells in one bit line have their drain terminals in common.

[0007] The programming or writing of an individual memory cell is based on the well-known phenomenon of hot electron injection. In essence, the cell programming is enabled by an injection of hot electrons into its floating gate.

[0008] Such hot electrons are generated in the chan-

nel of the floating-gate transistor, in the proximities of the drain region and in the presence of electric fields of such strength that the electrons are conferred a much different mobility from that due to their normal thermal agitation.

[0009] For the injection of electrons to take place, the electrons must be supplied kinetic energy of a greater magnitude than the potential energy existing between the channel and the gate region. This is achieved by biasing the gate and drain terminals of the memory cell at relatively high voltages, e.g. of 12.5V and 6.5V, respectively.

[0010] This biasing step involves considerable dissipation of current, and it is vital that the cell accessing resistors should produce no such voltage drops as may degrade the value of the bias voltage applied.

[0011] It is indeed well recognized that, for cells of the flash type, a reduced value of the drain voltage V_{pd} produces an insufficient or slow-rate cell programming.

[0012] On the other hand, too high a value of the drain voltage V_{pd} may give rise to destructive snap-back phenomena, or cause the cell to be soft-erased, i.e. become partially erased.

[0013] The optimum range for the drain voltage V_{pd} is, therefore, a fairly limited one, with variations on the order of 200mV to 300mV from a typical reference value dictated by the technology. The writing rate and snap-back phenomenon respectively set the lower and upper end points of the drain voltage variation range which is acceptable for correct programming of the cell.

[0014] Memory devices are provided with a sophisticated type of voltage regulator adapted to supply the bit lines of the cell matrix with an accurately regulated drain voltage during their programming step.

[0015] However, advanced miniaturizing technologies make it increasingly more difficult to provide programming circuitry which is capable of generating appropriate bias voltages. In fact, the reduced width and thickness of the interconnect lines result in higher resistance of the conduction paths used for applying the drain voltage to the memory cells. In addition, the current dissipation of each cell increases as a result of the reduced oxide thicknesses.

[0016] These problems become even more acute at the testing stage, when a plurality of cell are to be programmed in parallel and simultaneously in order to lower the cost and time for the operation. This results, in fact, in increased voltage drops across the conduction paths used for accessing the drain terminals of the cells.

[0017] Furthermore, the reduced channel length brought about by the ongoing miniaturization processes significantly restricts the variation range of the drain voltage, mainly on account of the lower snap-back voltage.

Background Art

[0018] A number of programming circuits are pro-

posed by the state of the art to solve these problems. For example, a typical solution is described in European Patent Application No. 93830545.5, wherein a drain voltage regulator has slightly higher output voltage than the desired voltage on the bit line.

[0019] The voltage difference is instantaneously dependent on the current actually flowing through the bit line select transistors.

[0020] A regulator of this type is formed by means of an adaptive bias technique using a positive feedback structure. This structure provides for the use of a "central" generator including an average voltage drop compensator for the access lines to the cell drains.

[0021] The voltage is regulated by means of a feedback circuit of the cascode-compensator type. In this case, however, an outer feedback loop also exists which modifies the system reference voltage according to the output current. Thus, the generator will supply a higher output voltage with larger output currents. This allows compensation of the voltage drop across the cell access lines. However, the bias variation due to the number of cells being programmed and their locations remains quite high.

[0022] While being advantageous in several ways, this prior solution applies its control action to the whole of the cells, and disallows a high programming parallelism effective to speed up the memory device testing procedure.

[0023] A more recent prior solution is described in another European Patent Application, No. 96830192.9, wherein local drain voltage generators are employed for each output sector of the memory matrix.

Figure 1 shows schematically an example of programming circuitry incorporating local generators of a drain voltage Vpd.

Figure 2 shows a more detailed electric diagram of the programming circuitry of Figure 1.

[0024] Vpp line represents the high-voltage supply for the programming step (Vpp=12.5V, for example).

[0025] In the circuitry shown in Figure 2, a reference voltage Vref is generated, usually as a division of the program voltage Vpp. This reference voltage Vref generally has a value of 6.5V which is "duplicated", with low output resistance, by the drain voltage Vpd generators. These generators locate adjacent to the memory matrix so that the access path to the cell drains is much shorter than in arrangements having a "central" generator and providing long signal distribution paths and transistors for accessing the matrix sectors which contain cells to be programmed.

[0026] In this second solution, moreover, the cell biasing is unaffected by how many and which output sectors happen to be involved in the programming. This also holds true for parallel programming, since it is possible to activate several independent paths at the output of

each generator by acting on column selection.

[0027] The circuit structure provided by this second solution comprises a negative feedback regulator which can smooth out the output voltage (Vyms) to a value close to the reference voltage (Vref) even at large output currents. The high differential gain of the comparator, the ample dynamic range of its output signal, and the high transconductance of the cascodes ensure regulation even in situations of considerable drift of the technological parameters and degradation of the supply voltage Vpp.

[0028] A capacitor at the comparator output is effective to create a dominant time constant in the feedback network which prevents overshooting at both the transient and the regulation phases.

[0029] Also provided are enable transistors controlled by a program signal, which inhibit the generator action when the data to be written into the cell correspond to the state of a virgin cell.

[0030] Even this second solution may be unsatisfactory where the resistance downstream of the generators becomes too high. For example, with very long bit lines, or where the current drain of the cells is quite large, as is the case with parallel programming, a voltage drop may occur across the whole of Vpp line resulting in the reference voltages being degraded.

[0031] The underlying technical problem of this invention is to provide a voltage regulator with such structural and functional features that the drain voltage Vpd during the programming step of plural memory cells can be held constant, thereby speeding up the memory device testing procedure and overcoming the aforementioned drawbacks which beset state-of-art solutions.

Summary of the Invention

[0032] The solving idea behind this invention is to provide for a suitably attenuated duplication of the output current Iout and to use the duplicated current Iout*α to modify the output voltage Vg of the comparator included in the regulator.

[0033] The technical problem is solved by a voltage regulator as previously indicated and defined in the characterizing portion of Claim 1 appended hereto.

[0034] The features and advantages of a regulator according to this invention will be apparent from the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

[0035] In the drawings:

Figure 1 shows schematically a programming circuitry for an electronic memory device incorporating a plurality of local voltage regulators;

Figure 2 is a more detailed diagram of the circuitry shown in Figure 1;

Figure 3 shows schematically an embodiment of a voltage regulator according to the invention, intended for incorporation to the circuitry of Figure 1.

Detailed Description

[0036] Referring in particular to the example of Figure 3, generally and schematically shown at 1 is a voltage regulator for suitably biasing the terminals of electrically programmable/erasable non-volatile memory cells, such as cells of the FLASH EEPROM type.

[0037] The cells are organized into a matrix 3 of the type formed of rows or word lines, and columns or bit lines. All the cells in one bit line have their respective drain terminals in common. A conventional row decoder 5 is associated with the matrix 3; also associated with the matrix 3 are a column pre-decoder 6 and its multiplexer 4.

[0038] The regulator 1 is particularly, but not exclusively, intended for a flash memory device comprising a cell matrix 3 divided into N sectors 7, e.g. sixteen sectors of at least one Mbit each and with memory words of sixteen bits.

[0039] There is one regulator 1 provided for each sector 7 of the memory matrix 3. The regulators 1 are similar constructions, and only one of them will be described hereinafter.

[0040] The invention provides for plural local regulators, each compensated for the output voltage drop.

[0041] The general construction of the programming circuitry to which the regulators 1 are incorporated is illustrated by Figures 1 and 2, which show substantially conventional circuit diagrams.

[0042] Each regulator 1 is powered between first Vpp and second GND voltage references. The first reference Vpp is a programming voltage of about 12.5V, to be applied to the word line of the cell matrix during the programming step. The second voltage reference GND is a signal ground.

[0043] The regulator 1 includes enable transistors and an operational amplifier 2 which is suitably feedback-connected to function as a comparator.

[0044] This comparator 2 has a first non-inverting input (+) which is applied a voltage reference Vref provided by a generator 8 effecting a division of the programming voltage Vpp.

[0045] Advantageously, the comparator 2 is controlled, as shown in Figure 3, by a programming step enable signal PG.

[0046] In detail, the comparator 2 comprises a pair of input MOS transistors MdrivR and MdrivY having respective source terminals connected together and connected to the ground GND through a transistor Me. The transistor Me receives a signal PG on its control ter-

minal which is produced from the output of an inverter 9 being input a negated signal PGn.

[0047] The comparator 2 is conventionally biased by a current mirror 11 connected between the supply Vpp and the aforesaid input transistors.

[0048] The comparator 2 of the regulator 1 has an output U connected by a line 13 to an output switch 15 which comprises an NMOS transistor Mcasc being a high transconductance cascode. A signal Vg is produced at the output U which is the outcome of the regulation performed by the comparator 2, as corrected according to the invention by a compensation block 20 to be described.

[0049] A smoothing capacitor Cstb and a discharge transistor Ms are respectively and independently connected between the output U and the ground GND. The transistor Ms receives the signal PGn on its control terminal.

[0050] The transistor Mcasc is connected to the supply Vpp by a cascode connection with a PMOS transistor MP having its body terminal connected to the supply Vpp and receiving the signal PGn on its control terminal.

[0051] The transistor Mcasc is further connected to a program line 10 connected to the bit lines of the memory matrix 3.

[0052] The line 10 is also connected to the second inverting input (-) of the comparator 2 which is coincident with the control terminal of the input transistor MdrivY. In this way, a feedback loop is provided.

[0053] The feedback loop, connected to the inverting input of the comparator 2, allows the value of Vreg to be smoothed according to the current drain from the line 10.

[0054] The construction of the compensation block 20 will now be explained.

[0055] This block 20 basically comprises a current mirror and a switch which is activated during the parallel programming step.

[0056] A first NMOS transistor Mirin is included in an input leg of a current mirror 16. This first transistor Mirin has its control terminal connected to the control terminal of the transistor Mcasc in the cascode switch 15.

[0057] The source terminal of the transistor Mirin is connected to the line 10.

[0058] The drain terminal of the transistor Mirin is connected to the supply Vpp through a series of a load transistor MdPP and a controlled transistor MswPP which is responsive to a signal PPn.

[0059] Both series transistors MdPP and MswPP are of the PMOS type with their body terminal connected toward the supply.

[0060] The control terminal of the load transistor MdPP is connected to the drain terminal of the transistor Mirin and, jointly therewith, to the output leg of the current mirror 16. In particular, a circuit node A connects the control terminals together of a PMOS transistor pair comprising an output transistor Mirout of the mirror 16

and a second load transistor Md.

[0061] The node A coincides with the drain terminal of the transistor Mirin and the drain terminal of the second load transistor Md. A voltage value Vcm_{ps} is present at the node A.

[0062] The source terminals of either transistors Mirout and Md are connected to the supply V_{pp}, while their respective body terminals are connected to the source terminals. Accordingly, both transistors are diode configured.

[0063] The drain terminal of the output transistor Mirout of the mirror 16 is connected to the connection line 13 going to the output U of the comparator 2. This transistor produces a current which is proportional by a parameter α to the output current I_{out} of the cascode 15.

[0064] The operation of the compensator 20 is based upon a suitably attenuated duplication of the output current I_{out} and the use of this duplicated current I_{out}* α to modify the output voltage V_g of the comparator 2.

[0065] The compensator 20 overcompensates the output current I_{out} by driving the cascodes such that the output resistance will be negative.

[0066] The operation of the compensator 20 will be described next in further detail.

[0067] The transistor Mirin operates as an input current mirror. In fact, since both transistors Mirin and Mcasc have similar source and gate bias and are operated in their saturation range, the currents they dissipate will be proportional to their dimensional ratio.

[0068] This enables the cascode current I_{out} to be mirrored with high attenuation. The input current to the compensator 20 is then converted to a voltage Vcm_{ps} by the second load transistor in diode configuration.

[0069] In the instance of a parallel programming step being carried out, the switch MswPP would be turned on by the signal Ppn and, accordingly, the first load transistor MdPP would be connected in parallel to the second load transistor Md.

[0070] The voltage Vcm_{ps} generates a current I_{out}* α through the output transistor Mirout operated in a saturated state.

[0071] Since the combination of the transistors Mirout, Md and Mdpp also form a current mirror, the outgoing current from the compensator 20 will be proportional to the cascode current I_{out}.

[0072] The attenuation factor has been previously indicated as the parameter α .

[0073] The current I_{out}* α generated by the compensator 20 alters the balance of currents at the output node U of the comparator 2, and increases the voltage V_g at the node U.

[0074] The current balance is restored as the voltage Yms at the output node OUT of the regulator 1 allows the corresponding input transistor MdrivY to take back in the compensation current I_{out}* α .

[0075] Assuming the differential gain of the comparator 2 to be infinite, for a given output current I_{out} the volt-

age at the node OUT Yms will be:

$$V_{yms} = V_{ref} + (\alpha/gm) * I_{out}$$

5 where, gm is the transconductance of the input transistors MdrivR, MdrivY of the comparator 2.

[0076] The compensation factor is arranged, as by appropriate dimensioning of the current mirrors, to cancel out the effects of the voltage drop across an access line of "standard" type. For memory cells located at the end of such a line, the following relation applies:

$$V_{drain} = V_{ref}.$$

15 [0077] The value of the compensation factor can now be expressed analytically. From relation:

$$V_{drain} = V_{ysm} - R_{drop} * I_{out}$$

20 with R_{drop} being the resistance of the line under consideration, it is:

$$V_{drain} = V_{ref} + (\alpha/gm - R_{drop}) * I_{out}$$

25 and therefore:

$$\alpha R_{drop} * gm$$

[0078] The compensation factor α would be modified, as mentioned, in the instance of parallel programming.

[0079] Using n to denote the number of cells to be programmed by a single regulator 1, the corrected output current to be considered for compensation is given as I_{out}/n.

35 [0080] This current can be obtained, according to the invention, in quite an equivalent manner by reducing the compensation factor α .

[0081] Thus, the parameter α to be used with parallel programming is given as α/n .

40 [0082] In the presence of very large output currents I_{out} or substantial drops in the voltage of V_{pp}, the transistors Mirin and Mirout of the mirror 16 are dimensioned, in the compensation circuitry, to exit their saturation range ahead of the transistors MdrivR and MdrivY of the comparator 2.

45 [0083] Thus, the performance of the regulator 1 becomes, under the above conditions, similar to that of an uncompensated regulator, thereby avoiding the instability problems which are typical of all circuits with a negative output resistance.

[0084] The voltage regulator of this invention does solve the technical problem and affords several advantages, foremost among which is an improved writing rate.

55 [0085] This reflects in superior efficiency during the write step and a shortened testing time. The programming parallelism made possible by the regulator of this invention is highly useful during the cell matrix testing.

The parallelism may indeed be enhanced to reduce selection time.

[0086] The regulator of this invention involves a limited increase in occupied area and constructional complexity over prior solutions.

[0087] In addition, using the regulator of this invention, the regulation is always applied locally, for each sector 7 of the matrix 3. In this way, the regulation is made independent of any voltage drops in the supply V_{pp} , as well as of the locations of the various circuit portions being programmed.

[0088] Modifications and variations may be made unto the regulator of this invention as the following claims may comprehend.

Claims

1. A compensated voltage regulator (1) useful with programming circuitry for electrically programmable non-volatile memory cells in a cell matrix (3) which is divided in sectors (7), said regulator being of a type which includes a comparator (2) connected between first (V_{pp}) and second (GND) supply voltage references, and having:
 - a first input terminal (+) which is supplied a by reference voltage (V_{ref});
 - an output terminal (U) connected to the control terminal of an output MOS transistor (M_{cas}) having a conduction terminal through which an output current (I_{out}) is passed and being connected to the memory cells by a program line (10);
 - a second input terminal (-), feedback connected to said program line (10); characterized in that it comprises a compensation block (20) powered from said first voltage reference (V_{pp}) and having an input connected to both said output terminal (U) and said output transistor (M_{cas}) and having an output connected to said output terminal (U) to generate a current (I_{out}· α) which is proportional to said output current (I_{out}) and attenuated with respect thereto by a predetermined α value, for supply to said output terminal (U).
2. A regulator according to Claim 1, characterized in that said compensator (20) includes a current mirror circuit (16) comprising an input transistor (Mirin) connected to said output transistor (M_{cas}).
3. A regulator according to Claim 2, characterized in that said input transistor (Mirin) and said output transistor (M_{cas}) have respective control terminals connected together and respective source terminals connected to said program line (10).
4. A regulator according to Claim 2, characterized in that said current mirror (16) further comprises an output transistor (Mirout) coupled to said input transistor (Mirin) through at least one load transistor (Md).
5. A regulator according to Claim 4, characterized in that the input (Mirin) and output (Mirout) transistors of said current mirror (16) are coupled together through at least one pair of load transistors in parallel with each other.
6. A regulator according to Claim 4, characterized in that the input (Mirin) and output (Mirout) transistors of said current mirror (16) are coupled together through at least one pair of load transistors which are adapted to be connected in parallel with each other by operation of a switch (M_{swPP}) controlled by a parallel programming enable signal (P_{pn}).
7. A regulator according to Claim 6, characterized in that said switch (M_{swPP}) is a PMOS transistor connected between a voltage supply reference (V_{pp}) and one of said load transistors (Md_{PP}).
8. A regulator according to Claim 4, characterized in that said at least one load transistor (Md) is in a diode configuration.
9. A regulator according to Claim 1, characterized in that the input (Mirin) and output (Mirout) transistors of said current mirror (16) are PMOS transistors.
10. Programming circuitry for a semiconductor integrated memory device having a matrix (3) of non-volatile memory cells, characterized in that it includes a regulator (1) according to Claim 1 for each sector (7) of the memory cell matrix (3).

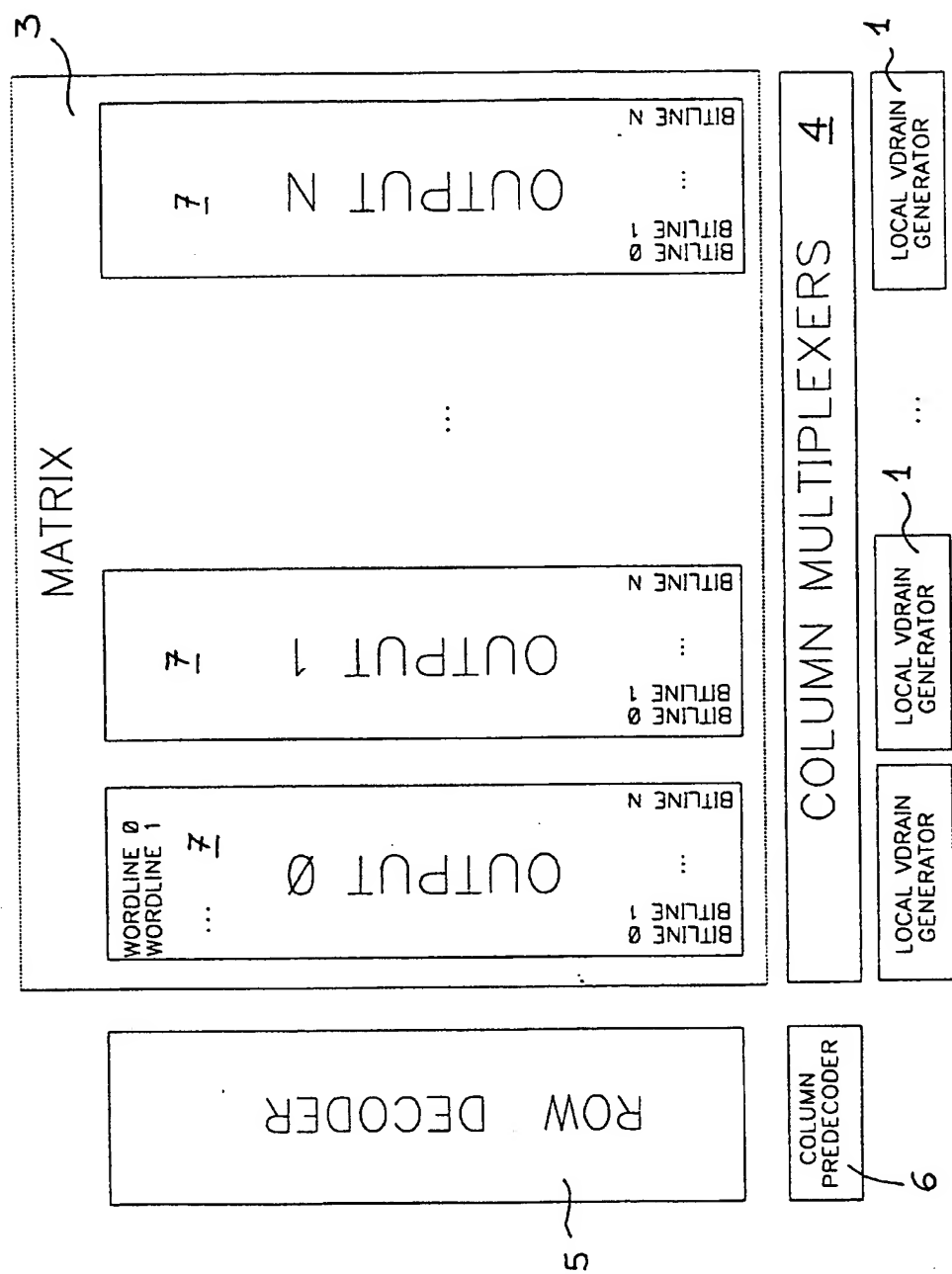


Fig. 1:

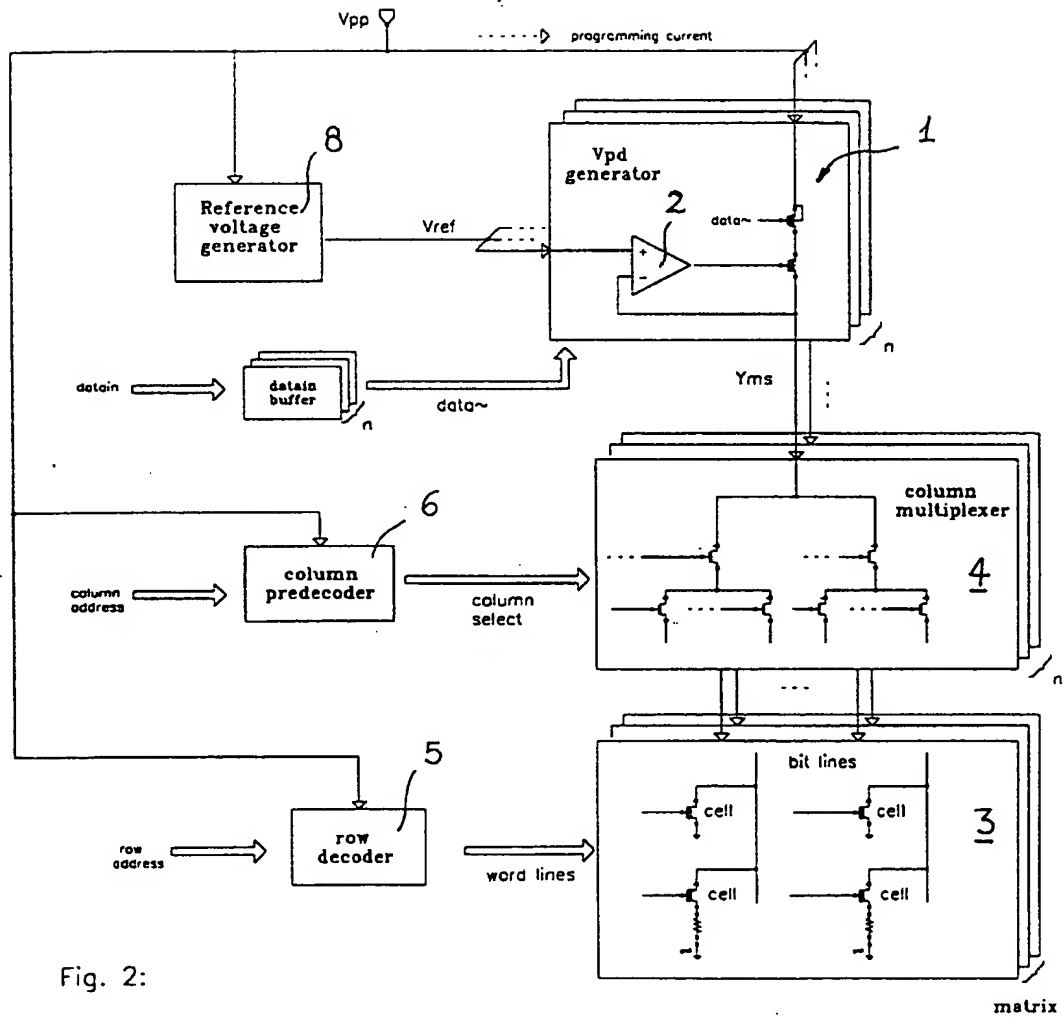
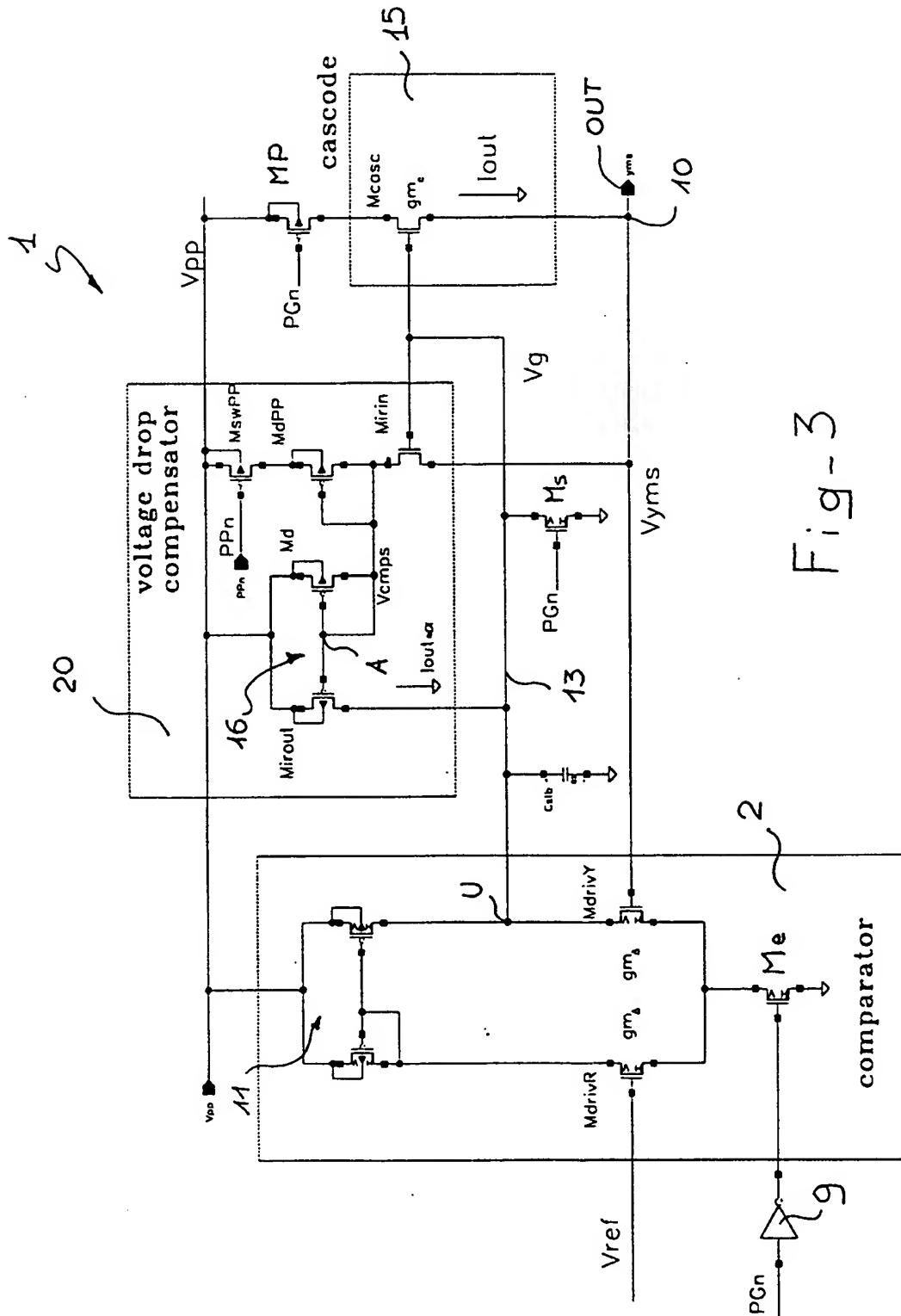


Fig. 2:





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Application Number

EP 97 83 0484

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|--|--|--|--|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
| D,A | EP 0 661 717 A (SGS-THOMSON MICROELECTRONICS SRL) 5 July 1995 * column 5, line 2 - column 7, line 23; figure 2 * | 1,2,9 | G11C16/06 G11C5/14 G05F3/26 |
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| | | | TECHNICAL FIELDS SEARCHED (Int.Cl.6) |
| | | | G11C G05F |
| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 29 June 1998 | Examiner Cummings, A |
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